ABSTRACT OF THE DISCLOSURE

What is disclosed is: a level transforming circuit comprising; a first CMOS circuit (10), a first intermediate circuit (30), a second intermediate circuit (40), a second CMOS circuit (20), a seventh p-channel type MOS transistor (51p), and an eighth p-channel type MOS transistor (52p); wherein the first intermediate circuit (30) and the second intermediate circuit (40) comprise a latch circuit. And, to this latch circuit, writing of data is performed by way of the seventh p-channel type MOS transistor (51p) and the eighth p-channel type MOS transistor (52p). Thus, a latch circuit is made up of CMOS inverter. Therefore, fast operation can be obtained and drop of drivability can be restrained.